UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,939	03/07/2001	Craig M. Perlov	10005727	6763

7590 07/31/2002

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	6

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,939	PERLOV ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *19-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 10005727-1
Filing Date: 3/7/2001
Claimed Foreign Priority Date: none
Applicant(s): Perlov et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the election (paper no. 5) filed on 5/13/2002.

Election/Restrictions

1. Applicant's election without traverse of claims 1-18 in paper no. 5 is acknowledged.

2. Claims 19-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-11 and 13-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Line 5 of claim 1 recites the limitation "each layer". There is insufficient antecedent basis for this limitation in the claim.

7. Line 5 of claim 1 recites the limitation "the layers of memory materials". There is insufficient antecedent basis for this limitation in the claim.

8. Lines 1-2 of claim 3 recite the limitation "the layers of memory materials". There is insufficient antecedent basis for this limitation in the claim.

9. Line 2 of claim 3 recite the limitation "each of the interfaces". There is insufficient antecedent basis for this limitation in the claim.

10. Lines 1-2 of claim 4 recite the limitation "the layers of memory materials". There is insufficient antecedent basis for this limitation in the claim.

11. Line 2 of claim 4 recites the limitation "each of the interfaces". There is insufficient antecedent basis for this limitation in the claim.

12. Line 1 of claim 5 recites the limitation "the layers". There is insufficient antecedent basis for this limitation in the claim.

13. Line 2 of claim 5 recites the limitation "the interfaces". There is insufficient antecedent basis for this limitation in the claim.

14. Line 2 of claim 11 recites the limitation "both sides of the center section substrate". There is insufficient antecedent basis for this limitation in the claim.

15. Lines 2-4 of claim 11 recite the limitation "the center section substrate". There is insufficient antecedent basis for this limitation in the claim.

16. Lines 1-2 of claim 13 recite the limitation "the memory materials on the first section". There is insufficient antecedent basis for this limitation in the claim.

17. Lines 2-3 of claim 13 recite the limitation "the memory materials on the second section". There is insufficient antecedent basis for this limitation in the claim.

18. Line 4 of claim 13 recites the limitation "the memory materials". There is insufficient antecedent basis for this limitation in the claim.

19. Lines 1-2 of claim 14 recite the limitation "the memory materials of the first and second sections". There is insufficient antecedent basis for this limitation in the claim.

20. Lines 1-2 of claim 15 recite the limitation "the first plurality of conductors". There is insufficient antecedent basis for this limitation in the claim.

21. Line 3 of claim 15 recites the limitation "the second plurality of conductors". There is insufficient antecedent basis for this limitation in the claim.

22. Lines 4-5 of claim 15 recite the limitation "the plurality of conductors on the second section". There is insufficient antecedent basis for this limitation in the claim.

23. Lines 5-6 of claim 15 recite the limitation "the plurality of conductors on the first section". There is insufficient antecedent basis for this limitation in the claim.

24. Lines 1-2 of claim 17 recite the limitation "the conductors of the first section". There is insufficient antecedent basis for this limitation in the claim.

25. Line 3 of claim 17 recites the limitation "the memory cells". There is insufficient antecedent basis for this limitation in the claim.

26. Lines 1-2 of claim 18 recite the limitation "the conductors in the second section". There is insufficient antecedent basis for this limitation in the claim.

27. Line 3 of claim 18 recites "the narrowing cross-section areas of the first section". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

28. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

29. Claims 1, 2, 4, 7, 8-12, and 15, are rejected under 35 U.S.C. 102(b) as being anticipated by Beilin (US 5854534).

30. Beilin shows all aspects of the instant invention including an assembly structure for a memory device, the structure comprising (see, *e.g.*, figs. 17A-17B):

- a substrate **602** having at least one fold line **612** thereon, dividing the substrate into at least two sections
- a layer **50'** of memory materials fabricated on each of the two sections

Beilin also shows adjacent sections of the layer **50'** forming an interface in which the memory materials are aligned to provide at least one operable electronic device **20** with the two sections folded on each other along the fold line (see, *e.g.*, figs. 1 and 3).

31. Regarding claim 2, Beilin shows the fold line **612** running approximately down the center of a definable portion of the substrate **602**.

32. Regarding claim 4, Beilin shows at least one **302** of the memory materials comprising conductor line patterns.

33. Regarding claim 7, Beilin shows the fold line **612** comprising one indentation in the substrate **602** (see, *e.g.*, fig. 17B).

34. Regarding claim 8, Beilin shows the fold line **612** comprising one crease in the substrate **602** (see, e.g., fig. 17B).

35. Regarding claim 9, Beilin shows that a property, of the substrate, *e.g.*, its width, changes along the fold line.

36. Regarding claim 10, Beilin shows two fold lines on the substrate **602**, providing three sections that fold over each other that may produce at least two active memory devices (col.5/ll.28-33).

37. Regarding claim 11, Beilin shows the three sections including a center section having a set of conductor lines that may be aligned with memory devices after folding the three sections one over each other (see, *e.g.*, fig. 16A and 19).

38. Regarding claim 12, Beilin shows an assembly structure for a memory device, the structure comprising (see, e.g., figs. 17A-17B):

- a common substrate **602** having multiple sections
- a first layer **50'** of memory material disposed on a first section of the multiple sections
- a second layer **50'** of memory material disposed on a second section of the multiple sections

- at least one fold line **612** disposed on the substrate defining an alignment of the memory materials on the first and second sections

Beilin also shows (see, *e.g.*, fig. 18) that the sections may be folded at the fold line **612** one over each other to form an operable electronic device.

39. Regarding claim 15, Beilin further shows

- a first plurality of conductors formed from an array of parallel conductors or wires spaces across the first section (see, *e.g.*, figs. 16A and 19)
- a second plurality of conductors formed from an array of parallel conductors or wires spaced across the second section (see, *e.g.*, figs. 16A and 19)

Beilin also shows the first plurality of conductors perpendicular to the second plurality.

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

42. Claims 3, 5, 13, 14, 17, and 18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Beilin in view of Maniar (US 5185689).

43. Regarding claim 3, Beilin shows most aspects of the instant invention (see paragraphs 30-38 above), except for the memory materials comprising semiconductor patterns. Beilin, however, shows a patterned capacitor structure **260** formed in at least one of the sections of the substrate (see, *e.g.*, fig. 2B).

Although Beilin fails to specify the materials for the capacitor structure, it is well known that polysilicon, which is a semiconductor, is a conventional material from which the capacitor electrodes of Beilin may be made of. See, for example, Maniar (col.3/ll.61-63), who teaches polysilicon as a conventional electrode material.

Accordingly, it would have been obvious to one of ordinary skill in the art to have at least one of Beilin's memory materials making of the capacitor structure comprising a semiconductor, as taught by Maniar, since semiconductor materials are conventionally used in the art as part of a capacitor structure.

44. Regarding claim 5, Beilin shows the memory materials comprising a plurality **302 304** of conductors. Beilin, however, fails to show the memory materials also comprising semiconductor patterns. Beilin, however, shows a patterned capacitor structure **260** formed in at least one of the sections of the substrate (see, *e.g.*, fig. 2B).

Although Beilin fails to specify the materials for the capacitor structure, it is well known that polysilicon, which is a semiconductor, is a conventional material from which the capacitor electrodes of Beilin may be made of. See, for example, Maniar, who teaches that polysilicon is a conventional electrode material (col.3/ll.61-63).

Accordingly, it would have been obvious to one of ordinary skill in the art to have the memory materials making up Beilin's capacitor structure comprising a semiconductor, as taught by Maniar, since semiconductor materials are conventionally used in the art as part of a capacitor structure.

45. Regarding claim 13, Beilin shows the first layer of memory material on the first section comprising a first plurality of conductor lines and the second layer of memory material on the second section comprising a second plurality of conductor lines (see, *e.g.*, fig. 16A and 19). Beilin, however, fails to show at least one of the layers also comprising semiconductor materials.

Beilin, however, shows a patterned capacitor structure **260** formed in at least one of the sections of the substrate (see, e.g., fig. 2B). Although Beilin fails to specify the materials for the capacitor structure, it is well known that polysilicon, which is a semiconductor, is a conventional material from which the plates of the capacitor structure may be made of. See, for example, Maniar (col.3/ll.61-63), who teaches polysilicon as a conventional plate material.

Accordingly, it would have been obvious to one of ordinary skill in the art to have a semiconductor among the memory materials making up Beilin's capacitor structure,

as taught by Maniar, since semiconductor materials are conventionally used in the art for a capacitor structure.

46. Regarding claim 14, Beilin fabricates the memory materials of the first and second sections so that, with the sections folded on each other along the fold line, the conductor lines and the capacitor structure are aligned to form the operable electronic device (see, e.g., figs. 1, 2B, and 18). As noted above in paragraph 44, the capacitor structure conventionally comprises semiconductor materials.

47. Regarding claim 17, Beilin shows the first section fabricated with narrowing cross-sectional areas (see, *e.g.*, fig. 17A).

48. Regarding claim 18, Beilin shows the second section including narrowing cross-sectional areas aligned with the narrowing cross-sectional areas of the first section (see, *e.g.*, figs. 18A-18B).

49. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beilin in view of Schantz (US 5453769).

50. Regarding claim 6, Beilin shows most aspects of the instant invention (see, *e.g.*, paragraphs 30-38 above), except for the fold line comprising a series of aligned perforations. Schantz (col.3/ll.4-7), on the other hand, teaches that having a series of perforations along the fold line can promote hinge formation along the fold line.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to have Beilin's fold line comprising a series of aligned perforations, as suggested by Schantz, in order to promote hinge formation along the fold line.

51. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beilin in view of Maniar and Chauvel.

52. Regarding claim 16, Beilin shows the first and second sections folded along the fold line so that the layers of memory material are in contact with each other (see, *e.g.*, fig. 18). As noted above in paragraph 44, Beilin shows that at least one of the sections includes a patterned capacitor structure **260** (see, *e.g.*, fig. 2B). Maniar, on the other hand, shows that semiconductor materials are conventionally used in the art as part of a capacitor structure.

In addition, Beilin shows that an IC chip **20** is formed on the folded first and second sections (see, *e.g.*, fig. 1). Beilin further teaches memory chips as conventional examples of IC chips (col.1/ll.46). As taught by Chauvel (col.1/ll.52-53), it is conventionally known that IC memory chips are semiconductor chips that consist of matrixes of memory cells distributed in rows and columns.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that any memory chip formed on the folded first and second sections of Beilin's assembly structure consists of semiconductor materials and patterns forming a matrix of memory cells, as taught by Chauvel, since it is conventionally known that IC memory chips are semiconductor chips that consists of matrixes of memory cells.

Conclusion

53. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814

Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

54. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

55. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

56. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/666-733,797	7/22/2002
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	7/22/2002

Marcos D. Pizarro-Crespo
Patent Examiner
Art Unit 2814
703-308-6558
marcos.pizarro@uspto.gov

MDP/mdp
July 24, 2002

SHEILA V. CLARK
PRIMARY EXAMINER